Integration of GaAsP on Si for High Efficiency Tandem Solar Cells

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ABSTRACT
Greater utilization of photovoltaic (PV) systems in utility-scale, aerospace, and military applications can be achieved by increasing module efficiency. Higher efficiency reduces the balance-of-systems and installation costs, comprising about half of utility-scale PV costs, since less area is required for a given power. Advances in aerospace and military PV technology, from unmanned vehicles to soldier-portable power, are dependent on increasing the specific power of PV modules which is attainable with efficiency improvements.

Crystalline Si (c-Si) currently dominates the PV market but its efficiency record is approaching the theoretically limiting efficiency. Multi-junction cells can be employed to improve efficiency above the single-junction Shockley-Queisser limit as achieved in III-V materials, but these typically are hindered by high costs. Integration of III-V and Si into a tandem (dual-junction) cell may offer an optimal combination of high efficiency and low cost. Maximum theoretical efficiency for a tandem with a Si bottom cell occurs with a top cell bandgap of ~1.7 eV. GaAsP (referred to as GaAsP) is an attractive top cell due to its direct and tunable bandgap in addition to the smallest lattice mismatch among ~1.7 eV materials.

My group has grown the highest efficiency GaAsP top cells to date relying on high-quality GaP/Si templates and compositionally graded GaAsP buffers. For this project, Crosslight TCAD software was utilized to simulate the device performance in comparison to experimental published work and explore the potential for improvement with increased material quality, decreased front reflection, and reduced top contact coverage. Simulations results predicted a pathway to a 20% efficient GaAsP top cell and therefore toward a 30% efficient tandem with c-Si, through a combination of design of an optimized anti-reflection coating, design of a top contact with 1% mesa coverage, electron minority carrier lifetime improvement to 1ns, and reducing parasitic loss from shunting.

1. INTRODUCTION AND MOTIVATION

Due to the detrimental effects of fossil fuels on the environment, the increasing United States and global energy demand requires a greater utilization of green energy. In some regions of the US, available photovoltaic (PV) technology is at “grid/socket parity”, where the cost of generating electricity to a wall plug with all factors considered is equal to or lower than the price of buying electricity from the grid. Spurred by the decreasing price of crystalline silicon for solar cells, installation of PV systems is greatly increasing. However, the balance-of-systems costs, including costs like labor and wiring, is now accounting for around 50% of the cost to generate electricity. Due to these non-module costs, improving module efficiency is a key factor to lowering cost by reducing the required area of a cell, and therefore reduce the necessary non-module costs for a given generation capacity. In addition to benefitting utility-scale power generation, increasing module efficiency can lead to high specific power PV technology where less weight is utilized for a given electricity generation. Specific power is critical for applications such as energy sources for satellites and unmanned aircraft to save launch fuel costs or as portable energy for the military.
The current utility-scale market for solar cells is dominated by crystalline silicon as multi-crystalline (multi c-Si) and single-crystalline (mono c-Si) account for 69% and 24% of global PV production respectively. The max theoretical efficiency of Si is 29.4% and mono c-Si record efficiencies of 26.6% and 24.4% were achieved for cell and module respectively. TABLE I compares current single-junction (SJ) record efficiencies for c-Si against record efficiencies of twenty years ago, showing the modest increase over this long time and the major reduction in ability to increase efficiency toward 29.4%. When factoring in the emphasis on increasing efficiency to decrease required non-module costs and the few percent of remaining record efficiency improvement for mono c-Si, potential for efficiency higher than 30% is critical for future acceleration of PV technology. Solar cells from GaAs achieved the highest single-junction efficiency of 28.8% (also shown in TABLE I), but are hampered by smaller substrate sizes and high substrate costs roughly a thousand times more expensive than Si substrates. Due to this high cost, GaAs solar cells typically are limited to applications such as space technology.

**TABLE I:** Comparison of single-junction (SJ) solar cell record efficiencies for current and 20 years ago under AM1.5G

<table>
<thead>
<tr>
<th>SJ Material</th>
<th>Current Cell&lt;sup&gt;a,b&lt;/sup&gt;</th>
<th>1997 Cell&lt;sup&gt;c&lt;/sup&gt;</th>
<th>Current Module&lt;sup&gt;a,b&lt;/sup&gt;</th>
<th>1997 Module&lt;sup&gt;c&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mono c-Si</td>
<td>26.6%</td>
<td>24.0%</td>
<td>24.4%</td>
<td>22.7%</td>
</tr>
<tr>
<td>Multi c-Si</td>
<td>21.3%</td>
<td>18.6%</td>
<td>19.9%</td>
<td>15.3%</td>
</tr>
<tr>
<td>GaAs</td>
<td>28.8%</td>
<td>25.1%</td>
<td>24.8%</td>
<td>N/A*</td>
</tr>
</tbody>
</table>

*No result for AM1.5G. Only result was measured under AM1.5D.

Multi-junction (MJ) solar cells are designed to surpass the SJ Shockley-Queisser limit for efficiency by more effectively converting higher energy photons to power using more than one junction with increasing bandgap. There are different approaches for combining junctions into a MJ structure including monolithic growth, wafer bonding, mechanical stacking, and spectrum splitting. GaAs is well-suited for monolithic growth due to multiple options for lattice-matched materials with relevant bandgaps. Again, the high GaAs substrate cost limits the application of GaAs MJ technology to high specific power markets and concentrator PV. Wafer bonding, mechanical stacking, and spectrum splitting are useful methods to overcome lattice-mismatch between junctions avoiding their challenging growth but incorporating extra complexity to the fabrication including layer transfer, four-terminal connections, and optics. These approaches are being utilized to better choose junction bandgaps closer to the optimum case for the number of junctions.

**FIGURE 1:** Predicted efficiency contour plots for an ideal tandem solar cell in series as a function of top and bottom cell bandgaps for (a) AM0 for space applications and (b) AM1.5 global for flat-plate applications. For both the red line shows the choice of a Si bottom cell. Adapted from Ref 7.

**FIGURE 1** shows the predicted efficiency of a dual-junction (tandem) solar cell structure connected in series. This indicates that a Si bottom cell with bandgap of 1.12eV and a top cell with a bandgap of
~1.7eV is near optimal for a tandem structure with either AM0 or AM1.5G spectra. III-V on Si tandems have the potential to achieve near theoretical efficiencies which is predicted to be 37-44% (depending on modeling assumptions). Due to the near ideal bandgap of Si for a tandem, potential ability to use a low-cost Si substrate, and vast industrial knowledge for Si solar cells, there has been research toward the integration of Si with other materials. TABLE II shows notable MJ and tandem record efficiencies with c-Si. The highest efficiencies were achieved with non-monolithic techniques due to the lattice-mismatch of Si with III-V materials as shown in FIGURE 2. A monolithic process would be preferred because it only requires a c-Si substrate and is less complex to manufacture into a cell/module. Perovskite has drawn large interest for a top cell material and is already demonstrating efficiency greater than 20% as a perovskite/Si tandem, but perovskite solar cells still need to demonstrate a much longer technology lifespan to be considered commercially. On the other hand, industries are already built depending on the demonstrated twenty-five plus year lifespans of many III-V materials and c-Si.

**TABLE II**: Record cell/submodule efficiencies for MJ with c-Si under AM1.5G

<table>
<thead>
<tr>
<th>MJ Materials (Top Cell/…/Bottom Cell)</th>
<th>Record Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaInP/GaInAs/Ge; Si (spectral split minimodule)</td>
<td>34.5%</td>
</tr>
<tr>
<td>GaInP/Si (mechanical stack)</td>
<td>30.5%</td>
</tr>
<tr>
<td>GaInP/GaAs/Si (wafer bonded)</td>
<td>30.2%</td>
</tr>
<tr>
<td>GaInP/GaAs/Si (monolithic)</td>
<td>19.7%</td>
</tr>
<tr>
<td>Perovskite/Si (monolithic)</td>
<td>23.6%</td>
</tr>
</tbody>
</table>

**FIGURE 2**: Bandgap as a function of lattice constant for III-V alloys and Si. Shows minimum energy bandgap (direct/indirect). Highlighted in red is the metamorphic growth pathway for the highest efficiency top cell grown on Si, as GaP is grown on Si and then compositionally graded to ~1.7eV GaAs$_x$P$_{1-x}$ as indicated by the black star. The horizontal dotted red line indicates ~1.7eV III-V material choices, while the vertical dotted red line indicates materials lattice-matched to ~1.7eV GaAs$_x$P$_{1-x}$.

All III-V candidates for a monolithic tandem with c-Si are lattice-mismatched causing reduced material quality from dislocations. This is demonstrated by the case of the monolithic triple junction GaInP/GaAs/Si where the record efficiency is less than the tandem GaInP/GaAs/Si cell by more than 10%. To account for lattice mismatch while attempting to minimize performance-limiting, metamorphic graded buffers are utilized to controllably alter the lattice constant of layers. GaAs$_x$P$_{1-x}$ is an ideal candidate for a top cell on c-Si because it has the smallest lattice mismatch among ~1.7eV III-V materials (as shown in FIGURE 2), a direct and tunable bandgap, and a transparent compositionally-graded buffer pathway from GaP. The current state-of-the-art for ~1.7eV GaAs$_x$P$_{1-x}$ (hereafter referred to as GaAsP) on c-Si with
11.5%–12.0% top cell efficiency was achieved by my current group. Key to its improvement over previous top cell was decreased by studying how buffer layer growth conditions affected the threading dislocation density (TDD) and by improving the device layer design. However further improvement of top cell material quality is required in addition to design and implementation of an anti-reflection coating (ARC) to make a GaAsP top cell which performs better than c-Si above ~1.7eV. To further the development of the GaAsP top cell and forecast its improvement with lower TDD and reduced reflection, this project simulates the performance of my group’s state-of-the-art device structure.

2. TECHNICAL BACKGROUND

A solar cell operates by the photovoltaic effect where an incident photon of light is absorbed in a material with a bandgap and excites an electron into the conduction band. Then due to diode junction asymmetry generated carriers can be separated and extracted from the diode as a photocurrent. This solar cell can be modeled through the ideal diode equation (EQUATION 1) or by including nonidealities through the double diode model (EQUATION 2). Circuit diagrams are shown in FIGURE 3 where the additional added elements are series resistance $R_S$, shunt resistance $R_{SH}$, and a second diode with slower current change with varied voltage.

\[
J(V) = J_L - J_0 \left[ \exp\left( \frac{qV}{n k_B T} \right) - 1 \right] \quad \text{EQUATION 1}
\]

Where $J_L$ is the generated light current density (for most cases $J_L = J_{SC}$ short circuit current density) and the second term represents ideal diode behavior when the ideality factor $n = 1$.

\[
J(V) = J_L - J_{01} \left[ \exp\left( \frac{q[V+J_AR_S]}{k_B T} \right) - 1 \right] - J_{02} \left[ \exp\left( \frac{q[V+J_AR_S]}{2k_B T} \right) - 1 \right] - \frac{V+J_AR_S}{A_{RSH}} \quad \text{EQUATION 2}
\]

Where the second term has $n = 1$ behavior, third term has $n = 2$ behavior, and the fourth term represents parasitic current loss through shunting. Additionally, voltage is dropped over series resistance with $I = J_A$. A double diode model is used to include both the effects of carrier recombination in the bulk material and at surfaces through $n = 1$ behavior and in the junction through $n = 2$ behavior.

![FIGURE 3](image)

A lighted current-voltage (LIV) curve can be obtained from sweeping the voltage in forward bias and measuring the current extracted from a solar cell under illumination. From an LIV curve the performance of a solar cell can be determined based on what are called “Figures of Merit” (FOM). FOM include short circuit current density $J_{SC}$, open circuit voltage $V_{OC}$, maximum power operation $P_{Max}$, fill factor $FF$, and efficiency $\eta$. The definitions for each are: $J_{SC}$ is the current density when $V = 0$, $V_{OC}$ is the voltage when $J = 0$, $P_{Max}$ is the maximum of the product $JV$, $FF$ is the ratio of $P_{Max}$ to the product $JSCVOC$, and $\eta$ is the ratio of $P_{Max}$ to incident light power. FOM determination is illustrated for an example LIV in FIGURE 4.
A solar cell material can extract the energy from absorbed photons more efficiently for photons with energies closer to its bandgap, since higher energy photons lead to thermalization. After high energy photons excite electrons to higher energy states in the conduction band, the electrons will thermalize to lower energy states by heating up the lattice. This reduces the electron potential energy that can be collected. Because of this MJ solar cells can improve the efficiency by cascading materials from higher energy bandgaps to lower bandgaps. The higher bandgap material will absorb higher energy photons and be transparent to photons below its bandgap. Then the next lowest bandgap material will absorb remaining photons above its bandgap and transmit below its bandgap, and so on. This is illustrated in FIGURE 5 as an example for a GaAsP on Si tandem. In a monolithic cascade, consecutive p-n junctions are connected in series by tunnel junctions, which operate as ohmic electrical contacts between n-type and p-type layers by introducing tunneling between the conduction band of the n-type layer and the valence of the p-type layer. For series connection of junctions, the current matching condition should be determined to design junction thicknesses, as being away from current matching will decrease the performance of the tandem by current limiting some of the junctions.

For monolithic growth of a III-V top cell on a c-Si bottom cell, several barriers need to be overcome for high material quality due to a polar/non-polar interface and lattice mismatch. The primary way that poor/highly defective material quality reduces device performance is through the introduction of trap states into the active region of the cell. The polar/non-polar interface can lead to anti-phase domains where instead of having all III atoms bonded to V atoms, some III atoms are bonded to III atoms. These III-III or V-V
bonds introduce trap states due to the altered local electronic environment. The formation of an APD is illustrated in FIGURE 6a-b along with how creating an atomic double-stepped surface for the IV substrate can lead to APD-free growth. Defect-free growth of GaP on Si has already been achieved and is utilized as a template for growth of the GaAsP top cell. Lattice mismatch primarily causes the growing layer to be strained and as the layer grows thicker more strain energy is stored up until a thickness where misfit and threading dislocations form to relax the material toward its lattice constant. Lines of dangling bonds are formed along the dislocations leading to trap states. Misfit dislocations are required to relax the material and occur along layer interfaces while threading dislocations extend up through the layer structure and can penetrate the active region of the cell to reduce performance. Misfit and threading dislocations are illustrated in FIGURE 6c. Dislocations will form in growing GaAsP layers as the layer needs to be thick to absorb sufficient light. The goal then of growth is to control the formation of dislocations to minimize the number of threading dislocations as long misfit dislocations from.

![FIGURE 6](image)

The trap states cause increased Shockley-Read-Hall (SRH) recombination by promoting transitions into the forbidden gap. SRH recombination decreases the number of carriers collected and reduces the quasi-Fermi level splitting. SRH recombination is illustrated against radiative recombination in FIGURE 6d. Minority carrier lifetime is the primary material parameter that is modified with the introduction of trap levels and SRH recombination. EQUATIONS 3-4 model the effect of threading dislocation density $[TDD]$ on the minority carrier lifetime $\tau$.^{11}

$$\frac{1}{\tau} = \frac{1}{\tau_{\text{Max}}} + \frac{1}{\tau_{\text{TDD}}}$$

_EQUATION 3_

Where $\tau_{\text{Max}}$ is the minority carrier lifetime in a threading dislocation-free material and $\tau_{\text{TDD}}$ is a threading dislocation density dependent parameter defined by EQUATIONS 4.

$$\tau_{\text{TDD}} = \frac{4}{\pi^3} D[TDD]$$

_EQUATION 4_
Where $D$ is the minority carrier diffusion coefficient. This model takes a threading dislocation as a local trap state which has an effective distance from its center where excess minority carrier concentration is decreased. For this model it is observed that for high TDD, $\tau$ will be dominated by the reduced $\tau_{TDD}$ term. This project simulates the effect of varying minority carrier lifetime on the GaAsP top cell performance.

To control the formation of dislocations, metamorphic growth utilizes graded buffers to slowly relax the layer to the desired active layer lattice constant. Then, the active layer can be grown lattice-matched to what is sometimes called a “virtual substrate”. Threading dislocation at the surface of the virtual substrate penetrate the active layer, but no new dislocations are created. Metamorphic growth is performed by epitaxial growth which allows the fine layer control of compositions, thicknesses, and interfaces along with growth condition control such as temperature and growth rate.

3. DEVICE STRUCTURE, DESIGN, AND SIMULATION RESULTS

To investigate the performance of the highest efficiency GaAsP top cell design on c-Si, simulations were performed in Crosslight TCAD software. The monolithic layer/device structure for the GaAsP top cell grown and fabricated by Yaung et al. is shown in FIGURE 7 alongside this project’s simulated structure. Some simplifications to the structure were used for ease of the simulation. These included combining the contact materials into single ohmic contacts including the highly doped GaAs contact layer used for both better ohmic contact and as a layer helpful for fabrication. Layers below the contact spreading layer (CSL) were not simulated due to the lower resistance of the CSL compared to the layer just below. Due to this the GaAs$_x$P$_{1-x}$ graded buffer layers, GaP buffer layers and c-Si p-n junction should not electrically affect the flow between contacts. Additionally, the composition of each layer for the simulation was determined by calculation of a 1.7eV GaAs$_{0.77}$P$_{0.23}$ p-n junction and lattice-matching the n-In$_{0.37}$Al$_{0.63}$P window layer and the p-In$_{0.35}$Ga$_{0.65}$P back surface field. The base layer thickness was chosen as 1.5μm as the higher efficiency device was achieved with this thickness.

![FIGURE 7: (a) ~1.7eV GaAsP top cell on c-Si layer structure with highest efficiency of top cell. (b) Layer structure used for simulations basing material composition as 1.7eV GaAsP and InAlP and InGaP lattice-matched to 1.7eV GaAsP. Layers below contact spreading layer (CSL) are neglected since only modeling top cell and CSL has lower resistance than graded buffer below. Doping levels are consistent with maximum achievable with our group’s Molecular Beam Epitaxy system.](image-url)
The layer structure design incorporates multiple elements intended to improve top cell performance. This includes a n-InAlP layer serving as both a window layer to direct minority hole diffusion away from the surface and toward the junction and as a partial contact spreading layer with its higher doping level. The InAlP window layer has a ~1.9eV indirect bandgap so that it contributes minimally to parasitic absorption since indirect materials have lower absorption coefficients. Next, a thin n-emitter is used to allow more absorption nearer to the junction and as hole mobility and diffusion length is generally lower than for electrons. A p-InGaP layer is used for the opposite purpose as the window layer, as it is a back surface field (BSF) which directs minority electron diffusion toward the junction. p-InAlP also be considered as a BSF material, but so far this structure has not been pursued. A CSL is in the layer design because it is desired to test only the GaAsP top cell without incorporating the influence of the c-Si bottom cell.

Below the CSL are GaAs,P, graded buffers from ~1.7eV GaAsP to GaP which have bandgaps greater than or equal to the top cell and even transitions from a direct to indirect material. Therefore, these layers are transparent to photons below ~1.7eV as needed for useful light to reach the c-Si bottom cell.
last III-V layer is the n-GaP nucleation layer which is critical to have APD-free growth and additionally will act as a window layer for the n-Si emitter when operating as a tandem cell. The last layer is the p-Si base which also acts as the substrate. Notable features missing from this layer structure include a tunnel junction as an ohmic electrical connection between junctions and an ARC which could improve the performance of this device by reducing front reflection. The current n-type electrical contact grid design also could be improved as it currently covers 8% of the top cell mesa.

The simulations of this project address the potential improvement for GaAsP top cell performance based on comparison relating to ARC and grid coverage. The performance gain from adding an ARC was simulated crudely by making a comparison between the layer structure with front reflection on or off. Even though this will not give the actual performance improvement with a well-designed ARC, the simulation should give simple results close to that achievable with an ARC. The grid coverage was simply compared by changing the n-contact width in comparison to the width of the mesa from the current coverage of 8% to an achievable 1% for a better grid design. Prior to these simulations, the minority carrier lifetime in the p-GaAsP base was varied to simulate LIV results similar to Ref 9. From this variation, a projection of the performance was determined with increased lifetime and therefore material with lower TDD. In order to

![Summary of “Figures of Merit” for LIV simulation results as a function of the electron minority carrier lifetime in the p-GaAsP base from 10ps to 1ns. FOM shown include (a) short circuit current density (b) open circuit voltage (c) fill factor and (d) efficiency. For each FOM the effect of simulating no front reflection and of changing the n-type top contact mesa coverage from 8% to 1%.](attachment:image.png)
achieve accurate solar cell simulations it was critical to have material complex refractive index. Complex refractive index data for ~1.7eV GaAsP and lattice-matched AlInP were obtained from recent results while the lattice-matched InGaP was less critical for these simulations as was further from top cell junction and was approximated by applying Vegard’s law to InP and GaP data.

Example simulated band diagrams are shown in FIGURE 8 under short circuit conditions with dark or with AM1.5G illumination to show the splitting of quasi-fermi levels due to the generation and collection of carriers. Of note is the length of the depletion width into the base due to the factor of ten difference between n-emitter and p-base doping. Additionally, the n-InAlP window layer results in a much higher barrier to minority carrier diffusion than the p-InGaP BSF. Results from the comparison of reflection with or without front reflection are shown in FIGURE 9 indicating that reflection losses of more than 25% over a wide photon energy range could potentially be utilized by the solar cell by implementation of a well-designed ARC coating. The design of an ARC coating will be difficult due to the necessity of accounting for a broadband spectrum to benefit both top cell and bottom cell. The reduction in reflection yields higher top cell absorption and increased $J_{SC}$ as shown in FIGURE 10a. In addition, lowering the reflection for photon energies less than ~1.7eV causes a large increase in the transmission of light through the top cell toward the bottom cell. FIGURE 10 shows that by reducing the n-type top contact coverage from 8% to 1% an increase in primarily $J_{SC}$ is achieved for improved efficiency. The effect of lower contact coverage is enhanced for the no front reflection case as a roughly 50% greater change in $J_{SC}$ was observed.

Simulation results are compared to experimental LIV data in FIGURE 11 where the experimental data is bound by a simulation of $\tau_n = 400ps$ with similar $J_{SC}$ and another simulation at $\tau_n = 75ps$ with similar $V_{OC}$ as a fit of both was not achieved on a single LIV curve. The fitting difficulty could have resulted if the simulation is not using a double diode model or is using a too small value of $J_02$ as the behavior near $V_{OC}$ for simulated against experimental is markedly different. Another very noticeable lack of the simulation model is the lack of shunting experimentally observed that reduced $FF$ by almost 10% from simulated.

![FIGURE 11: Comparison of simulated LIV curves and FOM to experimental LIV from Ref 9.](image)

This simulation project noted the multiple potential routes for performance improvement of the GaAsP top cell. Among these are material quality for longer minority carrier lifetime, design of an ARC, design of n-type top contact with lower mesa coverage, and decreasing parasitic losses to shunt resistance. As seen in FIGURE 10 the increase in $J_{SC}$ leads to the largest change in efficiency among the simulated
results. However, just improving the device design with an ARC and even with 1% n-type contact coverage supplementary improvements are need to increase the highest efficiency GaAsP top cell above 20% to make a 30% tandem feasible. Even though the simulation results for $\tau_n = 400\text{ps}$ with no front reflection and 1% contact coverage give $\eta = 20.8\%$ the fill factor factor reduction caused shunting would lead to about a 2% reduction in efficiency. However, improvement in material quality to $\tau_n = 1\text{ns}$ should be achievable as $\tau_n = 1.54\text{ns}$ was attained for p-GaAs grown on Si with SiGe buffers. When factoring improved material quality into the no front reflection and 1% contact coverage, simulations predict an $\eta = 21.9\%$ so 20% is achievable especially when working to reduce shunting through passivation.

4. SUMMARY AND CONCLUSIONS

As PV technology is breaking through in energy markets and applications, greater implementation is desired to meet the increasing energy demand and avoid the use of fossil fuel energy. Higher module efficiency can help to accelerate this process by requiring less area for a given generation capacity, thereby reducing non-module costs. In order to substantially increase module efficiency requires the use of multi-junction solar cells. MJ design structures typically result in high cost primarily due to the substrate. Therefore, integration of a MJ structure with c-Si is sought after to utilize the low-cost c-Si substrate and the vast industrial knowledge for c-Si solar cells. In order to best realize the cost benefit from c-Si, a monolithic approach should be pursued to avoid using expensive substrates.

A ~1.7eV top cell bandgap can achieve the highest theoretical efficiency tandem with a c-Si bottom cell, and GaAs$_x$P$_{1-x}$ is an attractive ~1.7eV top cell. GaAsP has the smallest lattice mismatch among ~1.7eV materials and a convenient transparent grading pathway from GaP to GaAs$_x$P$_{1-x}$ which is critical for metamorphic growth. Metamorphic growth by using buffer layers seeks to control nucleation of dislocations and reduce the effect of dislocations on minority carrier lifetime. My group has achieved the highest efficiency GaAsP top cells grown on Si with metamorphic growth.

Simulations with Crosslight TCAD software of this GaAsP top cell device structure were performed to compare to the highest experimentally-realized device. Additionally, the ability to increase device performance was investigated by simulating varied minority carrier lifetimes, front reflection, and n-type top contact coverage. Simulation results indicated that a 20% efficient GaAsP top cell is achievable through improvements in material and device quality by reduced threading dislocation density and less parasitic losses from shunting, careful design and implementation of an anti-reflection coating, and by reducing the mesa coverage. By realizing these advancements, designing and implementing a tunnel junction, optimizing the c-Si bottom cell for reduced degradation during III-V growth and for operation with the GaAsP filtered spectrum, and adjusting cell thicknesses and GaAsP composition for current matching a 30% efficient GaAsP on Si tandem may be realized.
REFERENCES