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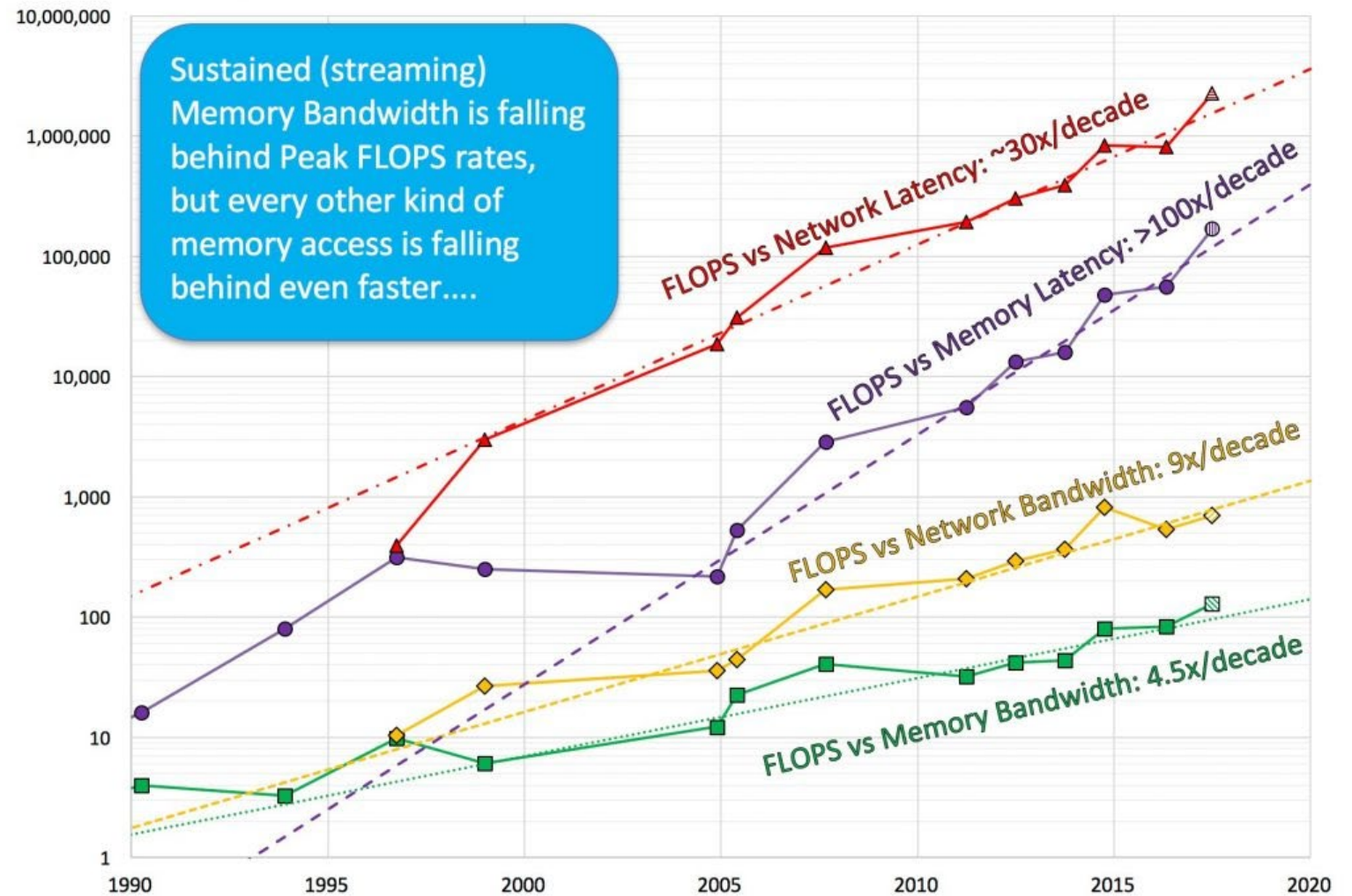
# High Frequency InGaN/GaN Micro LEDs for Optical Interconnect Applications

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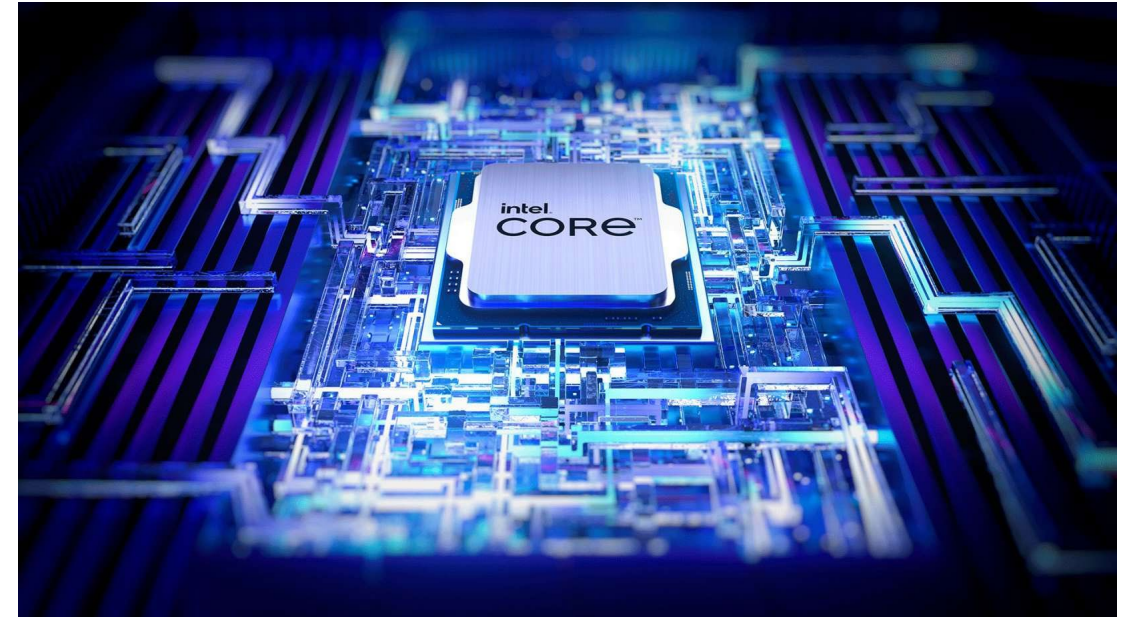
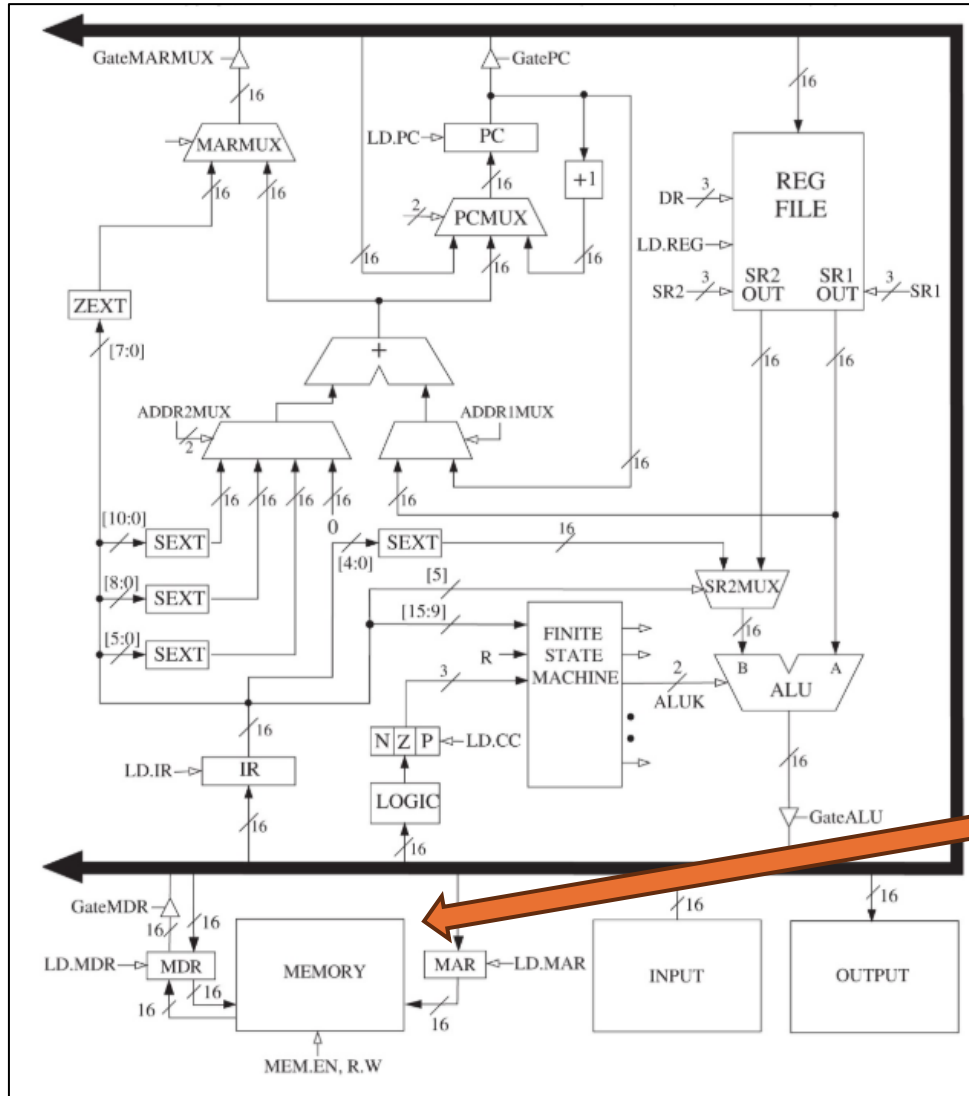
ECE443 – Spring 2024

Department of Electrical and Computer Engineering

- Memory and network speeds falling behind processing speeds
- Data transfers not keeping up

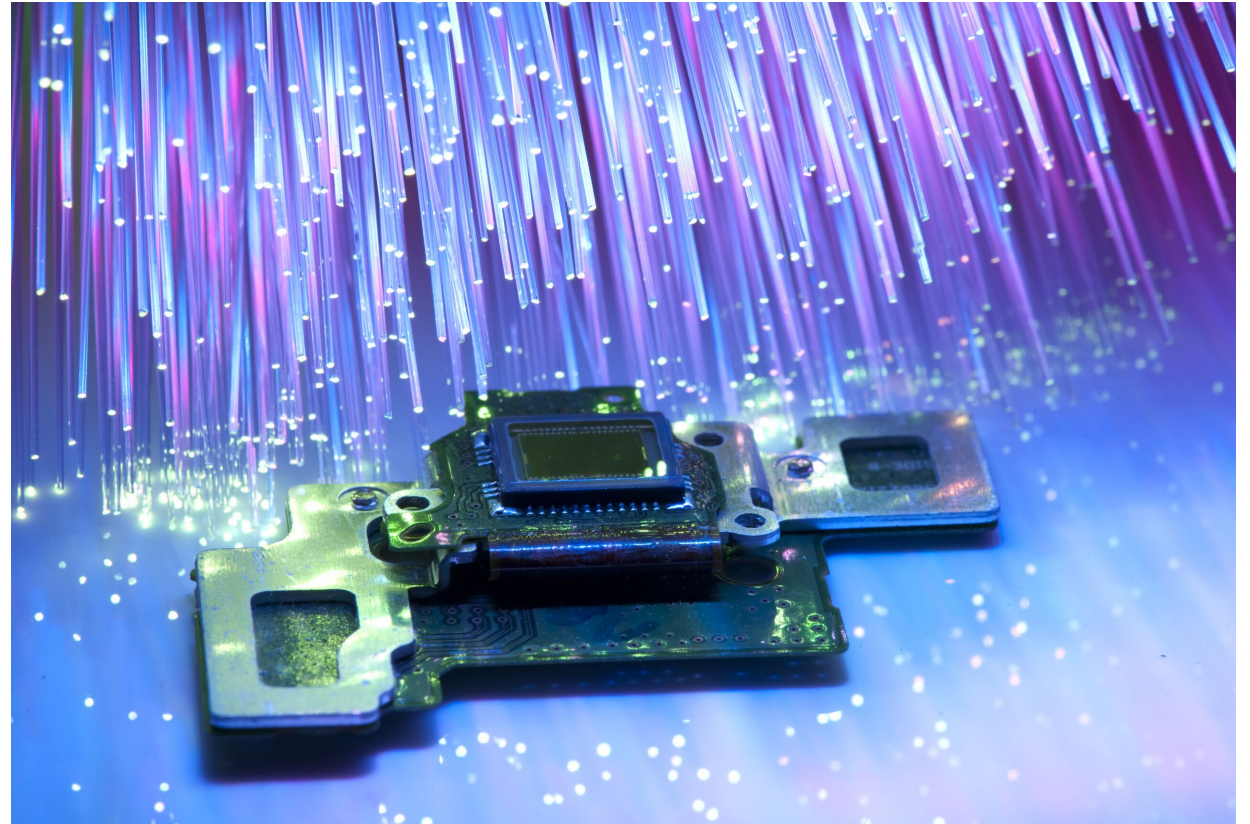


Flops versus data transfer speeds, John D. McCalpin 2016



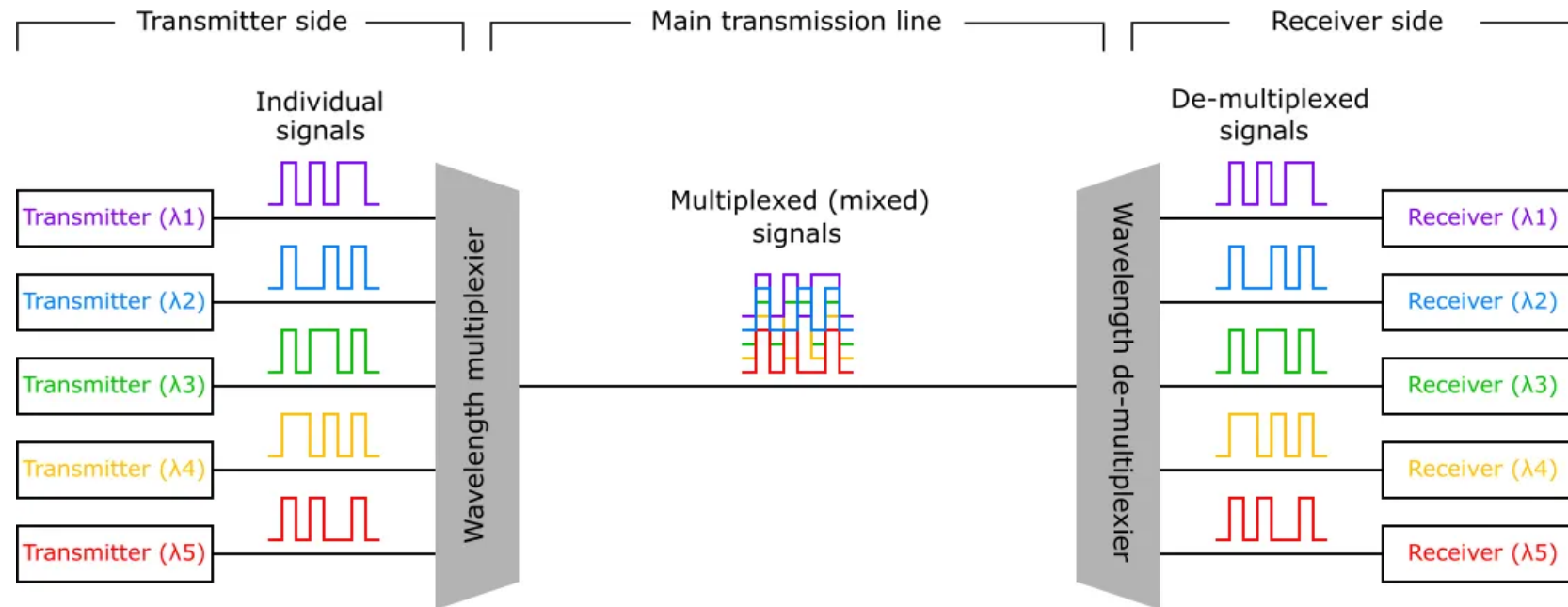
- Processors lose efficiency waiting for data from memory
- Takes a lot of energy for chip-to-chip, board-to-board interconnects

- **AI and computing have a large energy cost**
- **Increasing demand requires better data transfer methods**
- **Electrical interconnects are reaching theoretical limit**
- **Optical interconnects are potentially faster more robust**

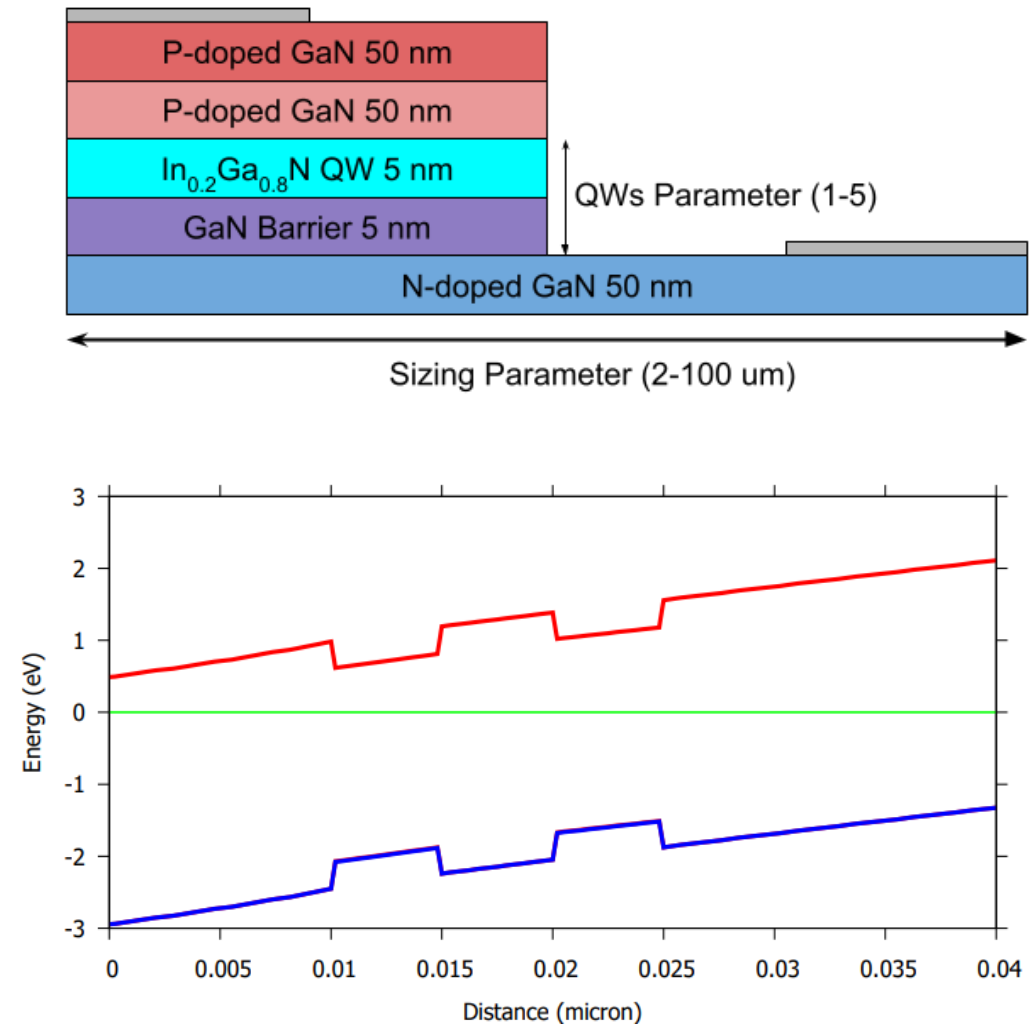


- **Properties of light allow for performance benefits**
  - **Separate wavelengths don't interfere, allows for WDM**
  - **Low attenuation over longer distances**

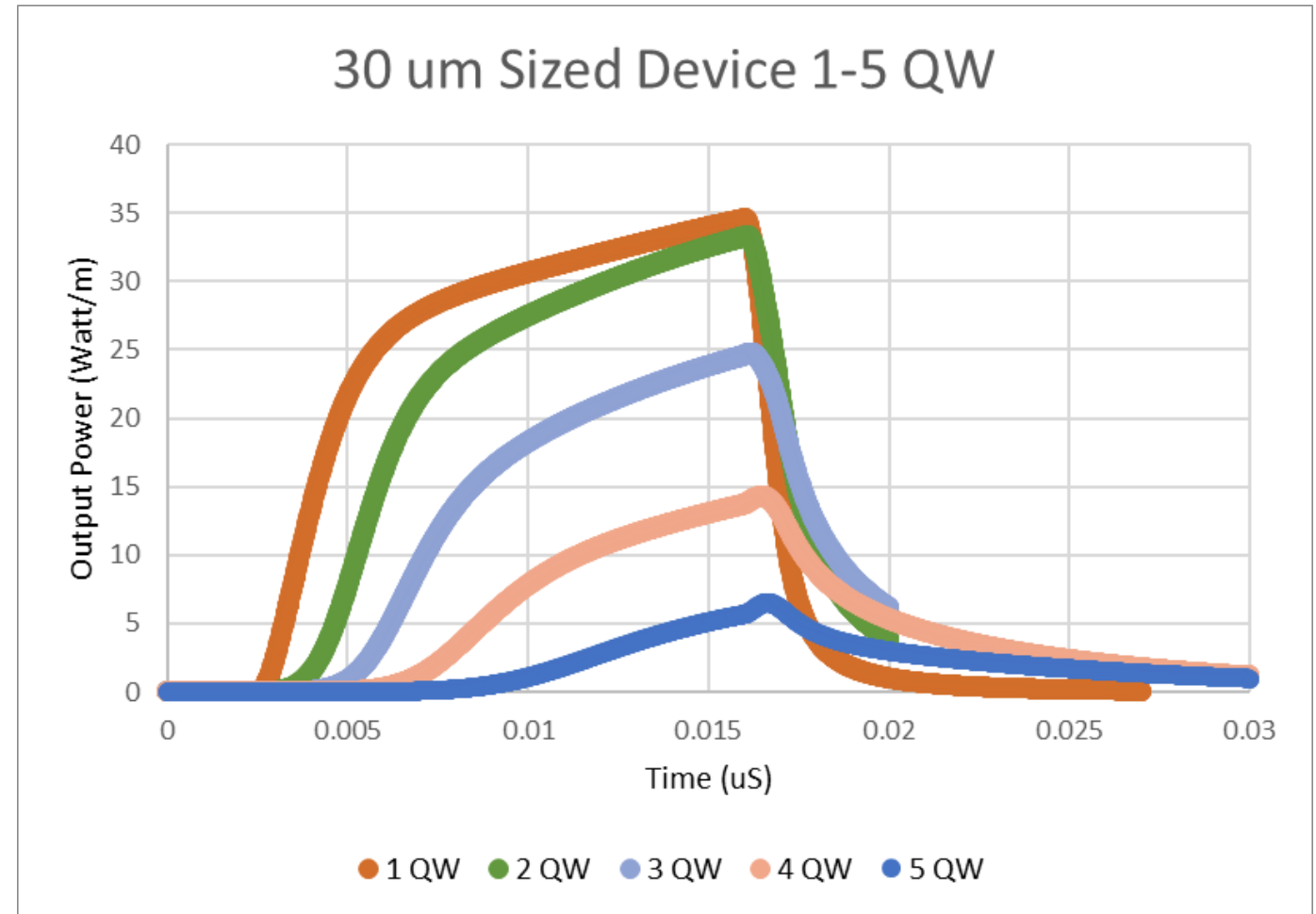
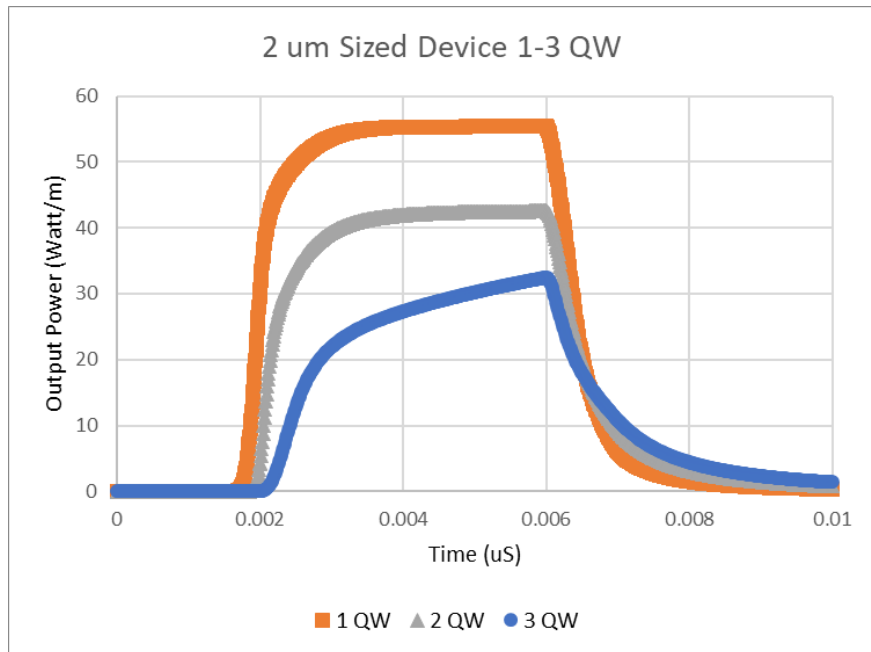
## Wavelength Division Multiplexing



- Target goal of 500 nm blue light
- InGaN/GaN quantum wells with doping
- Parameters:
  - Number of Quantum Wells
  - Sizing of device
- Important Metric:
  - Transient output power response time to input voltage pulse

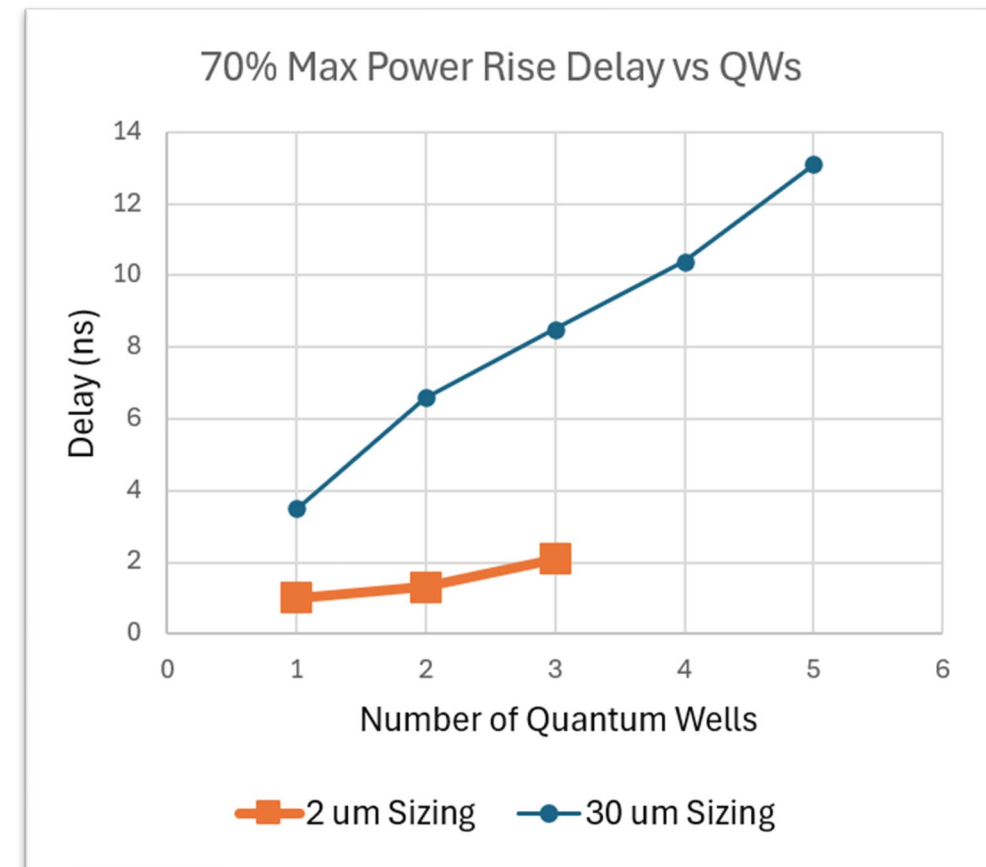


- Input voltage pulse on 30 um device with 1-5 QWs
- Input voltage pulse on 2 um device with 1-3 QWs
- Simulate transient output power



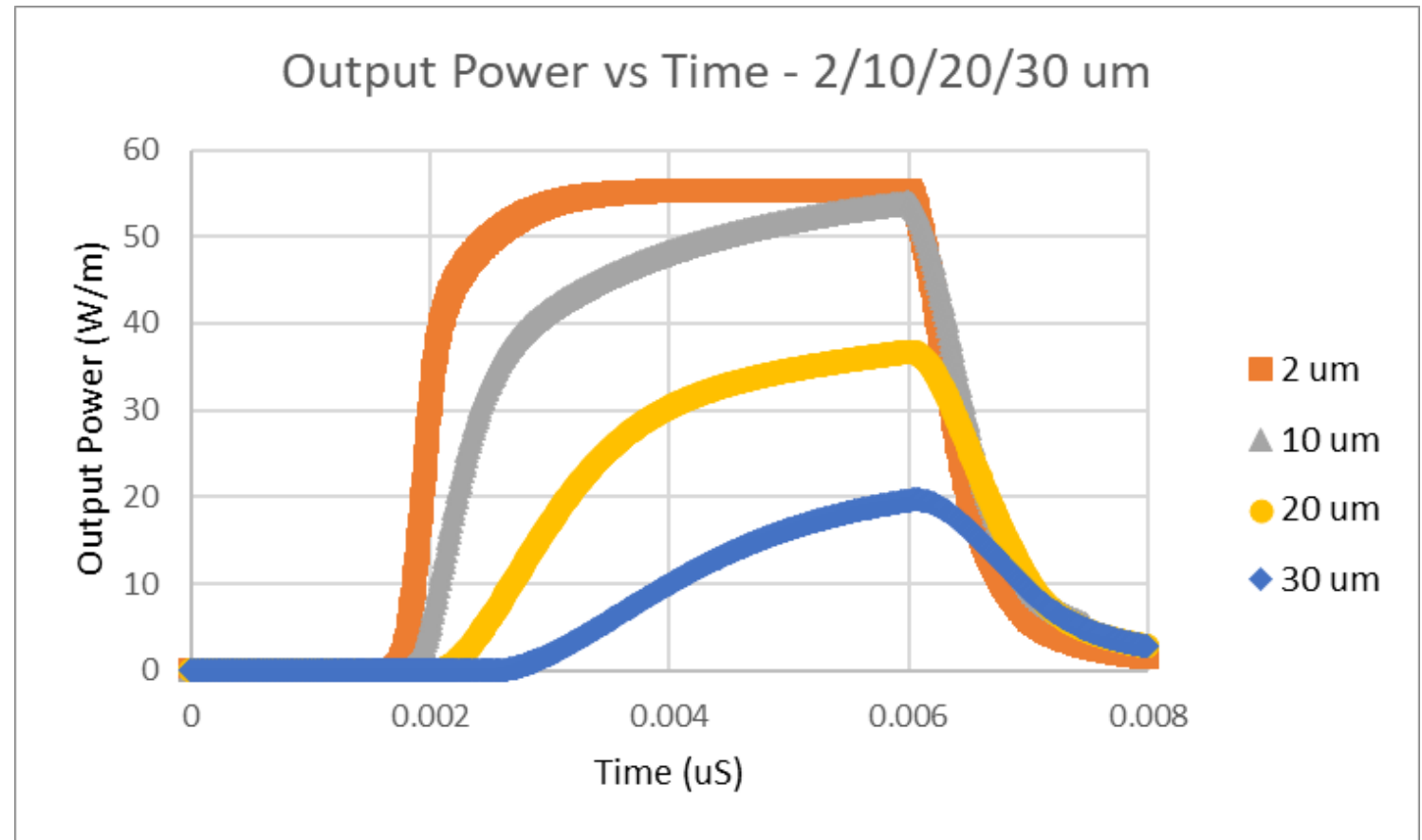
- As the number of QWs increases, the rise time also increases
- Graphing rise time vs #QW reveals a linear relationship
- Decreasing QWs increases frequency performance
- Tradeoff of low IQE and more droop

| 70% Rise Times  | 1 QW   | 2 QW   | 3 QW   | 4 QW    | 5 QW    |
|-----------------|--------|--------|--------|---------|---------|
| 2 $\mu$ m Size  | 1 ns   | 1.3 ns | 2.1 ns | NA      | NA      |
| 30 $\mu$ m Size | 3.5 ns | 6.6 ns | 8.5 ns | 10.4 ns | 13.1 ns |



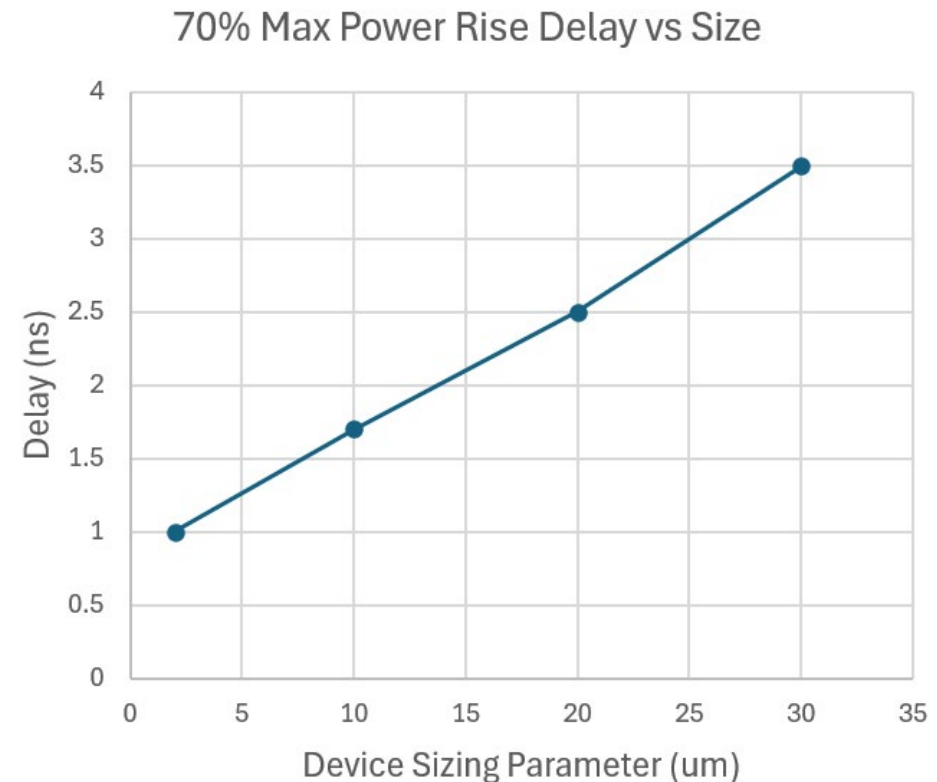


- Input voltage pulse on 1 QW device
- Change sizing parameter from 2  $\mu\text{m}$  to 30  $\mu\text{m}$
- Simulate transient output power



| 70% Rise Times | 2 um Size | 10 um Size | 20 um Size | 30 um Size |
|----------------|-----------|------------|------------|------------|
| 1 QW           | 1 ns      | 1.7 ns     | 2.5 ns     | 3.5 ns     |

- **As the number device size increases, the rise time also increases**
- **Graphing rise time vs device sizing again reveals a linear relationship**
- **Decreasing device size increases frequency performance**
- **Tradeoff of low IQE from surface recombination effects**



- **Decreasing the sizing of micro-LEDs and the number of quantum wells will increase frequency and switching ability**
- **There is a tradeoff with both approaches, leading to lower IQE and more droop inefficiency**
- **Micro-LEDs offer a new solution for data transfer if inefficiencies can be overcome, and operating frequencies can be increased**

**Thank You!**  
**Q & A**



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